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10/595,303	05/19/2006	Roy Knechtel	60291.000048	7114

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EXAMINER	
PARENDO, KEVIN A	
ART UNIT	**PAPER NUMBER**
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,303	KNECHTEL, ROY	
	Examiner	Art Unit	
	Kevin Parendo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2009 and 19 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-19* is/are pending in the application.

4a) Of the above claim(s) *11-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species I (claims 1-9) in the reply filed on 9/25/09 is acknowledged. The traversal is on the ground(s) that the inventions are not "independent and distinct" (page 6, paragraph 4) and that there is not a serious burden (page 7, paragraph 2). This is not found persuasive because the applicant is arguing restriction rules from chapter 800 of the MPEP (see "independent and distinct" arguments and quotations of MPEP 802.01, page 6, paragraph 4, MPEP 803, page 7, paragraph 2) regarding restriction practice in U.S. applications, not the rules regarding national stage applications of a PCT (see MPEP 1893.03d). Because this application is a national stage "371" application resulting from PCT/DE04/02413, these arguments are unpersuasive.

2. As discussed in the restriction requirement, as required by the PCT rule 13.1, the governing criteria is the "single general inventive concept rules". The species were properly identified (paragraph 1) and the lack of a single general inventive concept and lack of a common "special technical feature" were discussed (paragraph 4). The requirement is still deemed proper and is therefore made FINAL. Thus, claims 1-9 and 11-19 are pending and claims 1-9 will be examined.

Claim Objections

3. Claim(s) 1-9 is/are objected to because claim 1 contain(s) the limitation “processed semiconductor wafers" on lines 1-2, the limitation “more than two wafers” on line 4, the limitation “the wafers” on line 4, the limitation “semiconductor wafers” on line 7, “the limitation “the wafers" on line 12, and the limitation "the wafers" on line 13. These limitations all include the word “wafer,” and it is unknown if these limitations all refer to the same wafers or not. The claim language of the above limitations, and any instances of "wafer" in the dependent claims 2-9, must be brought into unambiguous agreement with each other. Appropriate correction is required.

4. Claim(s) 1 is/are objected to because it/they contain(s) the limitation “electrically non-conducting and electrically conducting glass paste" on lines 9-10 that should be amended to “electrically non-conducting glass paste and electrically conducting glass paste”. Line11 contains the limitation “the glass pastes" that lacks proper antecedent basis and that should be amended to "the electrically non-conducting glass paste and the electrically conducting glass paste. Lastly, claim 1 contains the limitation “the glasses of the glass pastes” on lines 13-14 that lacks proper antecedent basis. It appears that it should be amended to "the electrically non-conducting glass paste and the electrically conducting glass paste”.

5. Claim(s) 4, 5, and 8 is/are objected to because it/they contain(s) the limitation "the same processing temperature” (claim 4), “different processing temperatures” (claim

5), and “a temperature” (claim 8). These limitations must be brought into proper agreement with the limitation “processing temperature” in claim 1.

6. Claim(s) 9 is objected to because it/they contain(s) the limitation "the electric connection… is implemented through previously produced openings in a buried oxide layer and in an active silicon layer” is ambiguous as whether or not the openings are formed in the active silicon layer, or if the electric connection is formed in the active silicon layer. The limitation "the electric connection" on line 2 lacks proper antecedent basis and is ambiguous as to if it is one of the “electrically insulating connections” or one of the “electrically conductive connections” of the independent claims. Appropriate correction is required.

7. Claim 4 is objected to because the term "substantially" is a relative term (one definition of "substantial" is “being largely but not wholly that which is specified”) that renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation “a process for connecting processed semiconductor wafers, wherein, at least two wafers are located in a mid position of a stack of wafers, and wherein in an operation of a mechanical connecting, electrical insulating connections and electrically conductive connections are produced between at least two semiconductor wafers” on lines 1-7.

The metes and bounds of the claimed limitation can not be determined for the following reasons: it is unknown if “semiconductor wafers”, “the wafers”, “more than two wafers", and "processed semiconductor wafers" all refer to the same wafers, or if some limitations refer to the same set of wafers while other limitations refer to other wafers. **Claim 9** further describes a “substrate” and "a SOI wafer". The scope of these claims is not clear. One of ordinary skill in the art would not describe a "SOI wafer" (which has the structure of a semiconductor layer on an insulating substrate) as a "semiconductor wafer" (which is generally regarded as a simply slab of homogeneous semiconductor material). It is simply unclear if some or all of these are intended to refer to the same “wafer” or “wafers”.

The claim has the limitation “applying structured layers of electrically non-conducting and electrically conducting glass paste on two wafer sides of said two wafers to be connected”. This limitation is ambiguous as to the exact locations where

the structured layers are formed. Does “two wafer sides of said two wafers” require forming on only two sides total (i.e. two of the following sides: top of wafer #1, bottom of wafer #1, top of wafer #2, and bottom of wafer #2), or on both sides of each of wafers #1 and #2? Furthermore, it is unknown what a “structured layer” is. Does it mean that it is one layer that is made of "sub-layers" of the two types of paste? Does it mean that it is a layer that has "structures" in it?

Claims 2-9 depend from claim 1 and inherit its deficiencies.

9. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation “not structured electronically as an area of a starting material.” The metes and bounds of the claimed limitation can not be determined for the following reasons: the meaning of this limitation is unknown. It is unclear what a “starting material” of a wafer is.

10. In light of the aforementioned rejections of the claim(s) under 35 U.S.C. 112, second paragraph, the subsequent rejections under 35 U.S.C. 102 and/or 103 are based on prior art that reads on the interpretation of the claim language of the instant application as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The examination guidelines for determining obviousness under 35 U.S.C. 103 are described in MPEP 2141-2145.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,555,414 B1 ("Vanfleteren") in view of US 2004/0142540 A1 ("Kellar").

Re claim 1, Vanfleteren discloses a process for connecting processed semiconductor wafers **3** ("substrate" column 6, line 39) and **1** (alternatively called a "chip" column 6, line 41 and a "semiconductor chip", column 3, lines 51-55) wherein at least two wafers are located in a mid position of a stack of wafers, and wherein in an operation of mechanical connecting, electrically insulating connections (**5** provides electrically non-conducting, or insulating, connection, Fig. 4C) and electrically

conductive connections (**6** provides electrically conductive connection, Fig. 4C) are produced between at least two semiconductor wafers, said process comprising:

- applying structured layers of electrically non-conducting **5** (column 8, line 48 and Fig. 4C) and electrically conducting **6** (column 8, line 54 and Fig. 4B) glass paste (the electrically conducting adhesive is an “isotropically conducting adhesive", or ICA, which has a “glass transition temperature”, column 8, line 29) on two wafer sides (both **5** and **6** are first applied on the top side of the substrate **3**, Fig. 4C and then "on" the bottom side of 1 when **1** and **3** are joined together, see Fig. 4F) to be connected (they are not yet electrically connected until pressed together and thermally processed) with each other;
- conditioning and premelting (a “drying" process is conducted at 100 degrees; see column 8, lines 28-38; this occurs before curing, as can be considered “premelting” since “premelting” is not a standard term, and could either mean “melting before” but “before what” isn’t specified, or it could mean some heating that occurs before “melting” or “curing”) of the glass pastes;
- geometrical alignment (evolution from Fig. 4E to Fig. 4F) of the wafers to be connected; and
- joining (column 9, line 36) of the wafers at a processing temperature (column 9, lines 40-41) of the glass pastes using a mechanical pressure (column 9, line 39).

Vanfleteren does not disclose joining two semiconducting wafers. It is noted that the "applying…", "conditioning…", "geometrical alignment…", and "joining..." steps, the wafers that are processed are not claimed to be semiconducting. It is reasonable that the preamble is discussing joining a semiconducting wafer to another wafer, which may or may not be semiconducting. Vanfleteren discloses the second option, as the substrate **3** can be a printed circuit board, transparent substrate, polyimide, or ceramic.

In any case, Vanfleteren discloses joining a part of a semiconductor wafer (a chip) to a substrate. It would have been obvious to one of ordinary skill in the art to generalize this to joining a whole wafer to another wafer. For instance, Kellar discloses bonding together multiple semiconducting wafers (paragraph 5) such as "active device wafers" (paragraph 18) with a "bonding adhesive such as borophosphosilicate glass (BPSG)" (paragraph 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kellar to the invention of Vanfleteren. The motivation to do so is that the combination produces the predictable results of bonding semiconducting wafers (Mori, paragraph 5).

Re claim 2, Vanfleteren further discloses that the glass pastes are applied by a screen printing process (column 7, line 58, wherein the conductive adhesive is screen printed).

Re claim 3, Vanfleteren further discloses that the non-conducting glass paste and the electrically conducting glass paste have different conditioning and premelting conditions (non-conducting conditions: column 8, lines 50-54; conducting conditions: column 8, lines 27-31 and 45-47) and therefore the conditioning and premelting are

implemented successively in a respectively separate process (this follows from the different conditions, since both sets of conditions are fulfilled during the bonding process).

Re claim 4, Vanfleteren further discloses that the non-conducting glass paste and the electrically conducting glass paste have substantially the same processing temperature (column 9, lines 36-45).

Re claim 5, Vanfleteren further discloses that the non-conductive glass paste and the electrically conducting glass paste have different processing temperatures and these are successively passed in a process (column 9, lines 49-63).

Re claim 6, Vanfleteren further discloses that at least one of the two wafers is electrically connected in an area that is not structured electronically as an area of a starting material of the wafer (the wafer is connected between solder pads through adhesive **5**, Fig. 4F).

Re claim 7, Vanfleteren further discloses that the wafers are electrically connected at specific electric circuit points in electronically structured areas (the wafers are connected at solder pads **2A**, see Fig. 4F).

Re claim 8, Vanfleteren further discloses that a connection formation of the glass pastes takes place at a temperature in a range of 450*C (column 7, lines 64-65, column 8, lines 27-28, and column 9, lines 50-63).

12. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vanfleteren and Kellar as applied to claims 1 and 11 above, and further in view of US 2003/0170936 A1 ("Christensen").

Re claim 9, Vanfleteren discloses the limitations of claim 1, as discussed above, but fails to further disclose that the electric connection of a substrate of an SOI wafer is implemented through previously produced openings in a buried oxide layer and in an active silicon layer.

Christensen discloses that the electric connection of a substrate of an SOI wafer (paragraph 2) is implemented through previously produced openings **300** (Fig. 3 and paragraph 24) in a buried oxide layer **106 or 108** (Fig. 3) and in an active silicon layer **102** (Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Christensen to the invention of Vanfleteren. The motivation to do so is that the combination produces the predictable results of connecting a SOI wafer with improved speed of signals (Christensen paragraph 2) to an external wafer (Vanfleteren).

Response to Arguments

13. Applicant's arguments with respect to claims 1-9 have been considered but are not persuasive. In general, the applicants argue against the 112 rejection concerning a "structured layer" and say that it is a "term of art" (remarks, page 9, paragraph 1). The examiner disagrees. A search for this term returned very few results, mostly from

German references. The term is not a term of art. Perhaps what is more a term of art is “patterned layer”. The rejection is maintained.

14. Regarding the rejections for the many different names for “wafers”, the applicants dismiss any concern about the lax naming conventions. Statements in the remarks of a pending patent application do not define terms in the claims. Stating that "wafer", "two wafers", “at least two semiconductor wafers”, "semiconductor wafer", and “processed semiconductor wafer” are equivalent or refer to the same item(s) lacks support. The claim needs to be made to refer to the wafer or wafers with the same name throughout. Of course there is ambiguity when there is a "stack of wafers" as well. Claim 9 further describes a “substrate” and "a SOI wafer". The scope of these claims is not clear. One of ordinary skill in the art would not describe a "SOI wafer" (which has the structure of a semiconductor layer on an insulating substrate) as a "semiconductor wafer" (which is generally regarded as a simply slab of homogeneous semiconductor material). It is simply unclear if some or all of these are intended to refer to the same “wafer” or “wafers”. The applicants are encouraged to reconsider their statement that "our wording cannot be clearer, our wording can only be longer, but the scope of the claim would remain the same" (page 10, paragraph 3); this is an absurd statement considering how unclear it is to refer to "wafer" or "substrate" in about 6 or 7 different ways. If it really does not change the scope, then there is not reason not to make these terms agree with each other. The patent office does not charge any additional fee for extra words.

15. Regarding the "wafer sides", this is again not defined in the claims, and a discussion on page 8 does not define them.

16. The applicants argue against references individually, rather than what the combination of references would suggest. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The arguments against Kellar are not persuasive (see pages 9-10) because Vanfleteren and Kellar clearly disclose wafer bonding. Vanfleteren discloses flip chip bonding on substrates. It is quite obvious to one of ordinary skill in the art that these are interchangeable since the only difference is the specific material of the wafer (semiconductor) or substrate (ceramic, plastic, glass, or semiconductor). It is very common in the art to form semiconductor devices on either of these, and to bond these to other wafers, substrates, or holders.

17. The applicants further argue for "definitions" of terms that are not indeed terms of art of defined in the claims. They argue that it is an "unreasonably broad interpretation" to interpret as a “glass paste” a materials that has a “glass temperature” (see page 14-15). This is not persuasive. The term “glass paste” is quite ambiguous, and the claims never require that “a glass paste is not electrically conducting, but it is not the glue or adhesive 5… a glass paste does not need to be dried and cured, it is melted and pre-melted.” If that is what the applicant would like legal protection for, it needs to be claimed.

18. Lastly, the applicants argue that the invention is “surprising” and “astonishing” and has benefits of “simultaneous electrical connection” and “simultaneous sealing”.

The examiner notes though, that the claim language is very broad. It never requires “sealing”. It never requires processes to be "simultaneous". If these are unexpected and beneficial results, they should be claimed in order to differentiate over the prior art.

Conclusion

19. Applicant's amendment changed the scope of the claims and necessitated the new ground(s) of rejection presented in this Office action. Specifically, claim 1 previously required a structured layer on only one surface, and now it requires it on two. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Parendo, whose can be contacted by phone at

(571) 270-5030 or directly by fax at (571) 270-6030. The examiner can normally be reached on Mon.-Thurs. and alternate Fridays from 7 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin A. Parendo/
Examiner, Art Unit 2823
12/5/2009

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